IN THE CLAIMS

Please enter the following amendments to the claims. The amendments are believed to introduce no new matter.

1. (Original) A processor, comprising:

a plurality of registers;

processing circuitry associated with the plurality of registers, wherein the processing circuitry is operable to execute instructions included in a supported instruction set;

an instruction cache coupled to the processing circuitry, wherein the instruction cache is configured to provide copies of instructions in memory to the processing circuitry;

wherein a reset address line associated with the instruction cache is invalidated using reset address line invalidate circuitry upon reset.

2. (Original) The processor of claim 1, wherein reset address line invalidate circuitry invalidates a single line in instruction cache upon reset.

3. (Original) The processor of claim 1, wherein each line in the instruction cache comprises a tag portion and an instruction portion.

4. (Original) The processor of claim 3, wherein invalidating the reset address line associated with the instruction cache comprises setting the tag portion of the reset address line to invalid.

5. (Original) The processor of claim 4, wherein instructions from memory are copied into the instruction cache at the reset address line upon identifying the invalid state of the reset address line.

6. (Original) The processor of claim 5, wherein the tag portion includes the state of an instruction cache line.

7. (Original) The processor of claim 5, wherein the processor further comprises a data cache.

8. (Original) The processor of claim 7, wherein instructions copied comprise instructions for invalidating all other lines in the instruction cache.

9. (Original) The processor of claim 7, wherein instructions copied comprise instructions for invalidating all lines in the data cache.

10. (Original) The processor of claim 1, wherein the processor is a processor core on a programmable chip.

11. (Original) The processor of claim 10, wherein the processor is coupled to memory through a simultaneous multiple primary component fabric.

12. (Original) The processor of claim 10, wherein the processor can have its instruction cache invalidated upon reset without the use of bypass circuitry.

13. (Original) A programmable chip system, comprising:

processing circuitry associated with a plurality of registers, wherein the processing circuitry is operable to execute instructions included in a supported instruction set, the processing circuitry associated with reset address line invalidate circuitry operable to invalidate a line in processor cache;

a plurality of components coupled to the processing circuitry through an interconnection module.

14. (Original) The programmable chip system of claim 13, wherein reset address line invalidate circuitry invalidates a single line in instruction cache upon reset.

15. (Original) The programmable chip system of claim 13, wherein each line in the instruction cache comprises a tag portion and an instruction portion.

16. (Original) The programmable chip system of claim 15, wherein invalidating the reset address line associated with the instruction cache comprises setting the tag portion of the reset address line to invalid.

17. (Original) The programmable chip system of claim 16, wherein instructions from memory are copied into the instruction cache at the reset address line upon identifying the invalid state of the reset address line.

18. (Original) The programmable chip system of claim 17, wherein the tag portion includes the state of an instruction cache line.

19. (Original) The programmable chip system of claim 17, wherein the programmable chip system further comprises a data cache.

20. (Original) The programmable chip system of claim 19, wherein instructions copied comprise instructions for invalidating all other lines in the instruction cache.

21. (Original) The programmable chip system of claim 19, wherein instructions copied comprise instructions for invalidating all lines in the data cache.

22. (Original) The programmable chip system of claim 13, wherein the interconnection module is a simultaneous multiple primary component fabric.

23. (Original) The programmable chip system of claim 22, wherein the processor can have its instruction cache invalidated upon reset without the use of bypass circuitry.

24. (Original) A method for performing a reset, the method comprising:

identifying a reset event at a processor;

invalidating a reset address line associated with a processor cache;

obtaining a plurality of instructions from memory, the plurality of instructions obtained after a read access request for the reset address line;

executing a sequence of instructions to invalidate a plurality of lines associated with the processor cache.

25. (Currently Amended) The method of claim 1, wherein the reset address line ~~lien~~ is associated with a processor instruction cache.

26. (Original) The method of claim 1, wherein the sequence of instructions invalidates substantially all of the lines associated with processor cache.

27. (Original) The method of claim 1, wherein reset events are associated with hardware faults and software faults.

28. (Original) A processor, comprising:

means for identifying a reset event;

means for invalidating a reset address line associated with a processor cache;

means for obtaining a plurality of instructions from memory, the plurality of instructions obtained after a read access request for the reset address line;

means for executing a sequence of instructions to invalidate a plurality of lines associated with the processor cache.

29. (Original) The processor of claim 28, wherein the reset address lien is associated with a processor instruction cache.

30. (Original) The processor of claim 28, wherein the sequence of instructions invalidates substantially all of the lines associated with processor cache.